Ameba-Z Introduction

Outline

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- Power Saving Modes
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- BOR

Features

Features

Feature list		QFN68	QFN48	QFN32
Integrated core	Core type	ARM CM4		
	Core clock maximum freq.	125MHz		
Memory	Internal ROM	512KB		
	Internal SRAM	256KB		
	Max. External FLASH	128MB		
JTAG/SWD		SWD		
FPU	Float process unit	Yes		
XIP	Execute in place	Yes		
FPB	Flash patch breakpoint	Yes		
Backup register	Backup register for power save	16B		
Boot Reason	Reset reason	Yes		
Read protection	RAM read protection	4KB		
WIFI	802.11 B/G/N	Yes		
External 32K	External 32K	1		
Dsleep wakepin	Deep sleep wake pin	4		
BOR	Brown Out Reset Detection	Yes		

Features

Feature list			QFN68	QFN48	QFN32
peripherals	UART	Normal-UART Max. 6Mbps	2	2	1
		Log-UART Max. 6Mbps	1	1	1
	SPI Master	Max. 31.25Mbps	1	1	1
	SPI Slave	Max. 31.25Mbps	1	1	1
	I2C	Max. 400Kbps	2	2	2
	ADC	Battery Measurement: 0~5V	1	0	1
		Internal Thermal Measurement	1	1	1
		Normal channel: 0~3V	2	2	0
	GDMA	2*6 channels	2	2	2
	GPIO	IN/OUT/INT	39	26	17
	I2S		1	1	0
	RTC	D/H/M/S	1	1	1
		OUTPUT	1	1	1
	Timer	Basic timer (32K)	4	4	4
		Advanced timer (XTAL)	2	2	2
	PWM	OUTPUT	6	6	6
		INPUT Capture	2	2	2
	WDG		1	1	1
	USB device		1	0	0

SRAM

Free SRAM

CPU	Total	Free RAM	Usage
XXX_CPU	128K	50K	Data + heap
Ameba-I	512K	200K	Data + Heap + Text
Ameba-Z	256K	140K	Data + heap

Multi Cloud Support

application	Text	Data	Heap	XXX-CPU	Ameba-I	Ameba-Z
Alink 1.1 + 1SSL	60K+50K	28K	26K+14K	0	20K	72K
Joylink 1.3.3	61K	22K	14K	14K	103K	104K
Joylink 3.0	400K	70K		0	SDRAM	70K
Qqlink 1.1.101	70K	18K	26K	6K	86K	96K
Hilink 0.5.4	73K	13K	4K	33K	110K	123K
Gagent + Airkiss	77K	1K	21K	28K	101K	118
Weichat 3.1.0	89K	22K	13K	15K	76K	105K

Flash Controller

Flash Controller

- Execute in place (XIP)
  - Supports a memory-mapped I/O interface for read operation, which makes it in the same way as Ram read operation.
  - Support FPB
- Read cache:
  - 32KB I/D Read Cache
  - 16-Byte Cache line
  - 2-Way associative
- Address
  - 0x08000000, (Ameba1 is 0x98000000)
- Baud rate
  - 100/83/71/62/50MHz …
- SPI mode:
  - SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI
- Many types of flashes from multiple vendors have been supported in ROM
  - MXIC/GD/winbond/Micron

Flash AVL

Vendor	Part Number	Density	Voltage	IO
MXIC	MX25L1633E	2MB	3.3V	4IO
MXIC	MX25L3236F	4MB	3.3V	4IO
MXIC	MX25L6433F	8MB	3.3V	4IO
MXIC	MX25L12845G	16MB	3.3V	4IO
Winbond	W25Q80DV	1MB	3.3V	4IO
Winbond	W25Q16DV	2MB	3.3V	4IO
Winbond	W25Q32FV	4MB	3.3V	4IO
Winbond	W25R64FV	8MB	3.3V	4IO
Winbond	W25R128FV	16MB	3.3V	4IO
Micron	N25Q032A13ESE40E	4MB	3.3V	4IO
Micron	N25Q064A13ESED0E	8MB	3.3V	4IO
Micron	N25Q128A	16MB	3.3V	4IO
Micron	N25Q00AA13GSF40F	128MB	3.3V	4IO
Gigadevice	GD25Q80C	1MB	3.3V	4IO
Gigadevice	GD25Q16C	2MB	3.3V	4IO
Gigadevice	GD25Q32C	4MB	3.3V	4IO
Gigadevice	GD25Q64C	8MB	3.3V	4IO
Gigadevice	GD25Q128C	16MB	3.3V	4IO

XIP Performance

CPU performance

- CPU Performance

CPU	CPU clock	XIP	dhrystone	coremark
XXX_CPU	166MHz	Y	0.66	1.564
Ameba-I	166Mhz	N	0.77	1.367
Ameba-Z	125MHz	Y	0.96	1.710

WIFI performance

- High Performance Scenario

AP	Chipset	Security	Throughput (unit: Mbps)					
			TX			RX		
			XXX_CPU	Ameba-I	Ameba-Z	XXX_CPU	Ameba-I	Ameba-Z
TPLINK TL-WR2041N	Atheros	open	6.79	29.3	25.3	10	24	20.2
		AES	6.75	29.4	24.9	9.74	23.9	20.4
TPLINK TL-WDR4310	Atheros	open	7.06	30.4	25.3	10.4	25.7	21.2
		AES	6.85	29.5	23.4	9.61	24.2	20.1
ASUS RT-AC87U	Quantenna	open	5.8	29.6	25.5	9.78	25.4	21.4
		AES	8.27	29.3	24.1	7.91	24.7	20.6
XIAOMI mini-R1C	MTK	open	7.19	30.1	25.2	10.2	24.6	20.6
		AES	7.1	29.7	24	9.94	23.9	19.7
Netgear R7000	Broadcom	open	8.67	29.4	25.3	9.97	25.3	20.6
		AES	6.87	29.1	24.1	9.26	24.2	19.7
DLINK Dir-880L	Broadcom	open	8.93	29.3	25.2	10	24.8	20.6
		AES	8.06	28.4	24	9.86	24.1	19.6

WIFI performance

- More Free RAM Scenario

AP	Chipset	Security	11N		11G		11B	
			TX	RX	TX	RX	TX	RX
TPLINK TL-WR2041N	Atheros	OPEN	10.1	8.55	9.96	8.5	4.53	3.06
		AES	10.2	8.56	10.2	8.67	4.68	4.52
TPLINK TL-WDR4310	Atheros	OPEN	12.1	12	11.4	12.6	4.91	4.62
		AES	11.8	13.1	10.6	11.4	4.85	4.65
ASUS RT-AC87U	Quantenna	OPEN	15.3	14.2	11.8	13.1	N/A	N/A
		AES	15.3	13.8	13.5	13.4	N/A	N/A
XIAOMI mini-R1C	MTK	OPEN	12	9.98	N/A	N/A	N/A	N/A
		AES	12.2	9.98	N/A	N/A	N/A	N/A
Netgear R7000	Broadcom	OPEN	15.8	14.3	15	14.2	N/A	N/A
		AES	14.8	13.6	14.4	13.7	N/A	N/A
DLINK Dir-880L	Broadcom	OPEN	15.7	14.2	N/A	N/A	N/A	N/A
		AES	14.6	13.6	N/A	N/A	N/A	N/A

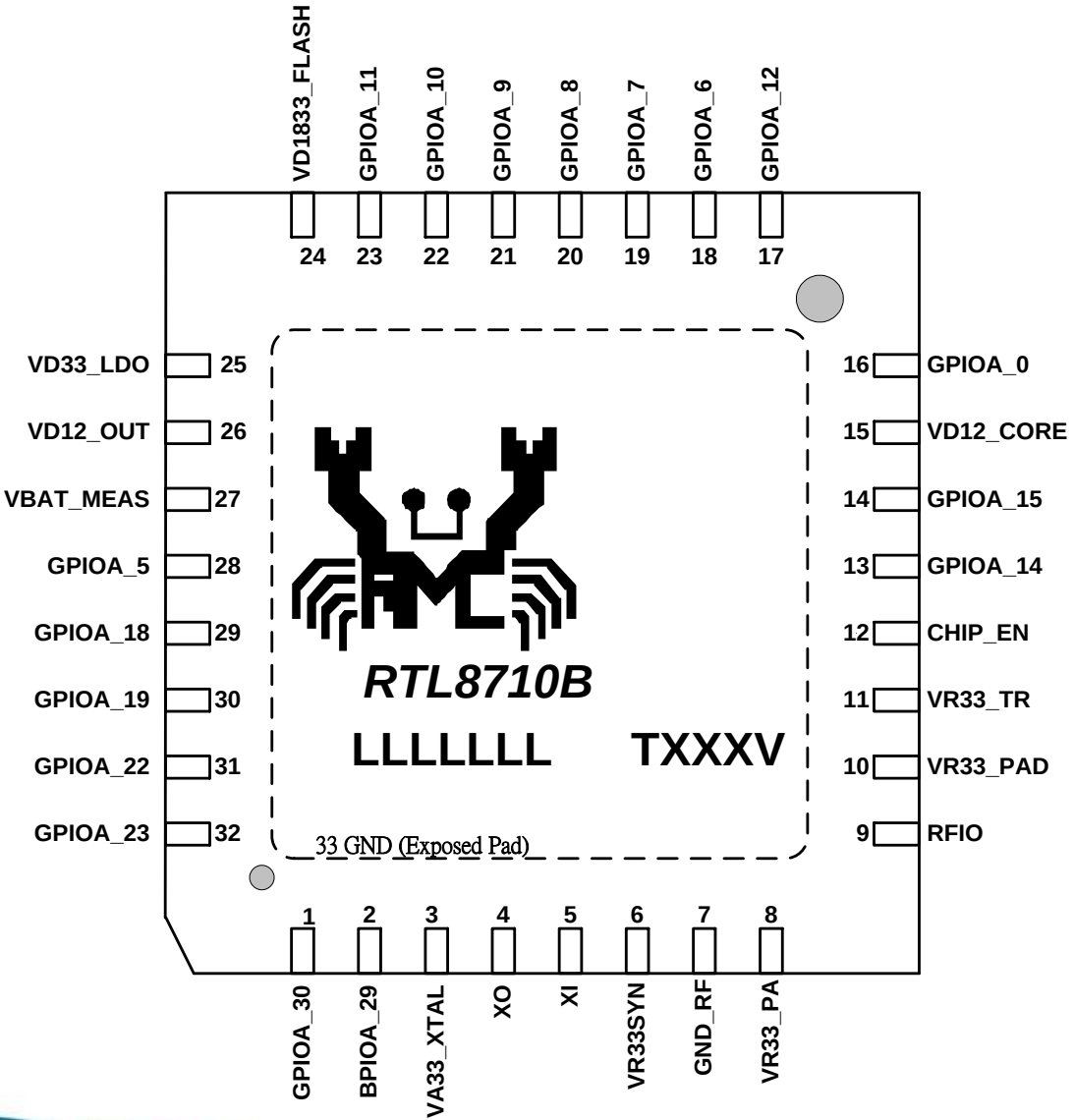
WIFI performance

- More Free IO Scenario

SPI Mode / Flash Clock	4 Bit Mode		2 Bit Mode	
	TX	RX	TX	RX
100M	10.1	8.5	9.7	8.5
83M	10.0	8.5	9.5	8.2
71M	9.8	8.5	9.2	8.2
62M	9.7	8.4	9.2	8.0
50M	9.5	8.4	8.8	7.6

Pin Assignment

Pin Name




```
/* (((port)<<5)|(pin)) */
typedef enum {
    PA_0  = (PORT_A<<5|0),
    PA_1  = (PORT_A<<5|1),
    PA_2  = (PORT_A<<5|2),
    PA_3  = (PORT_A<<5|3),
    PA_4  = (PORT_A<<5|4),
    PA_5  = (PORT_A<<5|5),
    PA_6  = (PORT_A<<5|6),
    PA_7  = (PORT_A<<5|7),
    PA_8  = (PORT_A<<5|8),
    PA_9  = (PORT_A<<5|9),
    PA_10 = (PORT_A<<5|10),
    PA_11 = (PORT_A<<5|11),
    PA_12 = (PORT_A<<5|12),
    PA_13 = (PORT_A<<5|13),
    PA_14 = (PORT_A<<5|14),
    PA_15 = (PORT_A<<5|15),
    PA_16 = (PORT_A<<5|16),
    PA_17 = (PORT_A<<5|17),
    PA_18 = (PORT_A<<5|18),
    PA_19 = (PORT_A<<5|19),
    PA_20 = (PORT_A<<5|20),
    PA_21 = (PORT_A<<5|21),
    PA_22 = (PORT_A<<5|22),
    PA_23 = (PORT_A<<5|23),
    PA_24 = (PORT_A<<5|24),
    PA_25 = (PORT_A<<5|25),
    PA_26 = (PORT_A<<5|26),
    PA_27 = (PORT_A<<5|27),
    PA_28 = (PORT_A<<5|28),
    PA_29 = (PORT_A<<5|29),
    PA_30 = (PORT_A<<5|30),
    PA_31 = (PORT_A<<5|31),

    PB_0  = (PORT_B<<5|0),
    PB_1  = (PORT_B<<5|1),
    PB_2  = (PORT_B<<5|2),
    PB_3  = (PORT_B<<5|3),
    PB_4  = (PORT_B<<5|4),
    PB_5  = (PORT_B<<5|5),
    PB_6  = (PORT_B<<5|6),
    PB_7  = (PORT_B<<5|7),
    PB_8  = (PORT_B<<5|8),

    // Not connected
    NC = (uint32_t)0xFFFFFFFF
} ? end PinName ?  PinName;
```

Per-pin Configurable

QFN68	QFN48	QFN32	GPIO	UART	SPI Master	SPI Slave	SPI Flash	I2C	SDIO	PWM/TIMER	EXT32K	I2S	Others
✓	✓	✓	PA_14							PWM0	SWD_CLK		
✓	✓	✓	PA_15							PWM1	SWD_DATA		
✓			PA_13							PWM4			
✓	✓	✓	PA_0							PWM2	ext_32K		
✓	✓		PA_16	UART2_log_RXD						PWM1	RTC_OUT		
✓	✓		PA_17	UART2_log_TXD						PWM2			
✓	✓		PA_25	UART1_RXD									
✓	✓		PA_26	UART1_TXD									
✓			PA_28					I2C1_SCL					
✓			PA_27					I2C1_SDA					
✓		✓	PA_12							PWM3			
✓	✓		PA_4	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C0_SDA					
✓	✓		PA_1	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C0_SCL					
✓	✓		PA_2	UART0_CTS	SPI1_CS	SPI0_CS		I2C1_SDA					
✓	✓		PA_3	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C1_SCL					
✓	✓	✓	PA_6				SPIC_CS		SD_D2				
✓	✓	✓	PA_7				SPIC_DATA1		SD_D3				
✓	✓	✓	PA_8				SPIC_DATA2		SD_CMD				
✓	✓	✓	PA_9				SPIC_DATA0		SD_CLK				
✓	✓	✓	PA_10				SPIC_CLK		SD_D0				
✓	✓	✓	PA_11				SPIC_DATA3		SD_D1				
✓	✓	✓	PA_5						SDIO_SIDEBAND_INT	PWM4			WAKEUP_1
✓	✓	✓	PA_18	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C1_SCL	SD_D2	TIMER4_TRIG		I2S_MCK	WAKEUP_0
✓	✓	✓	PA_19	UART0_CTS	SPI1_CS	SPI0_CS		I2C0_SDA	SD_D3	TIMER5_TRIG		I2S_SD_TX	ADC1
✓	✓		PA_20						SD_CMD			I2S_SD_RX	ADC3
✓	✓		PA_21						SD_CLK	PWM3		I2S_CLK	
✓	✓	✓	PA_22	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C0_SCL	SD_D0	PWM5		I2S_WS	WAKEUP_2
✓	✓	✓	PA_23	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C1_SDA	SD_D1	PWM0			WAKEUP_3
✓			PB_1		SPI1_CLK	SPI0_SCK							
✓			PB_0		SPI1_CS	SPI0_CS							
✓			PB_2		SPI1_MISO	SPI0_MISO							
✓			PB_3		SPI1_MOSI	SPI0_MOSI							
✓			PB_4								SWD_CLK	I2S_MCK	
✓			PB_5								SWD_DATA	I2S_SD_TX	
✓			PA_24									I2S_SD_RX	
✓			PA_31									I2S_CLK	
✓			PB_6									I2S_WS	
✓	✓	✓	PA_30	UART2_log_TXD				I2C0_SDA		PWM3	RTC_OUT		
✓	✓	✓	PA_29	UART2_log_RXD				I2C0_SCL		PWM4			

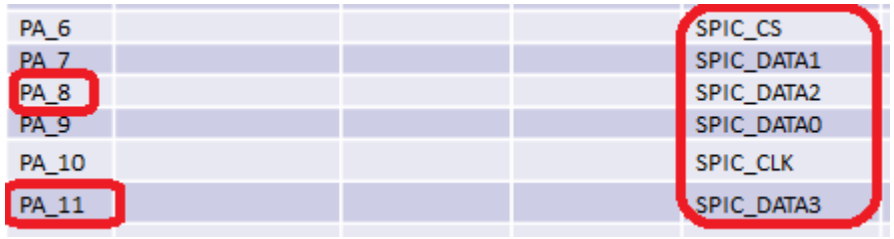
Per-pin Configurable

- UART0 RTS-CTS can be configured as I2C or GPIO, when RTS-CTS is not used

PA_4	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C0_SDA
PA_1	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C0_SCL
PA_2	UART0_CTS	SPI1_CS	SPI0_CS		I2C1_SDA
PA_3	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C1_SCL
PA_6				SPIC_CS	
PA_7				SPIC_DATA1	
PA_8				SPIC_DATA2	
PA_9				SPIC_DATA0	
PA_10				SPIC_CLK	
PA_11				SPIC_DATA3	
PA_5					
PA_18	UART0_RXD	SPI1_CLK	SPI0_SCK		I2C1_SCL
PA_19	UART0_CTS	SPI1_CS	SPI0_CS		I2C0_SDA
PA_20					
PA_21					
PA_22	UART0_RTS	SPI1_MISO	SPI0_MISO		I2C0_SCL
PA_23	UART0_TXD	SPI1_MOSI	SPI0_MOSI		I2C1_SDA

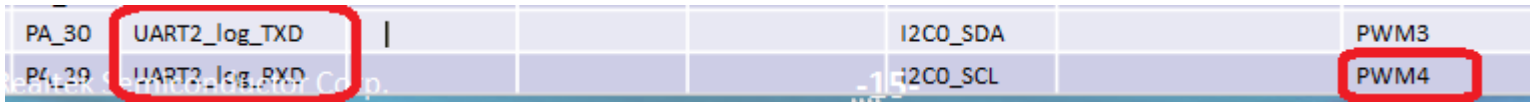
Per-pin Configurable

- Flash D2 & D3 can be configured as GPIO, when flash 2-bit mode used



PA_6				SPIC_CS		
PA_7				SPIC_DATA1		
PA_8				SPIC_DATA2		
PA_9				SPIC_DATA0		
PA_10				SPIC_CLK		
PA_11				SPIC_DATA3		

- UARTLOG RX can be configured as PWM, if UARTLOG TX is not used



PA_30	UART2_log_TXD				I2C0_SDA	PWM3
PA_29	UART2_log_RXD				I2C0_SCL	PWM4

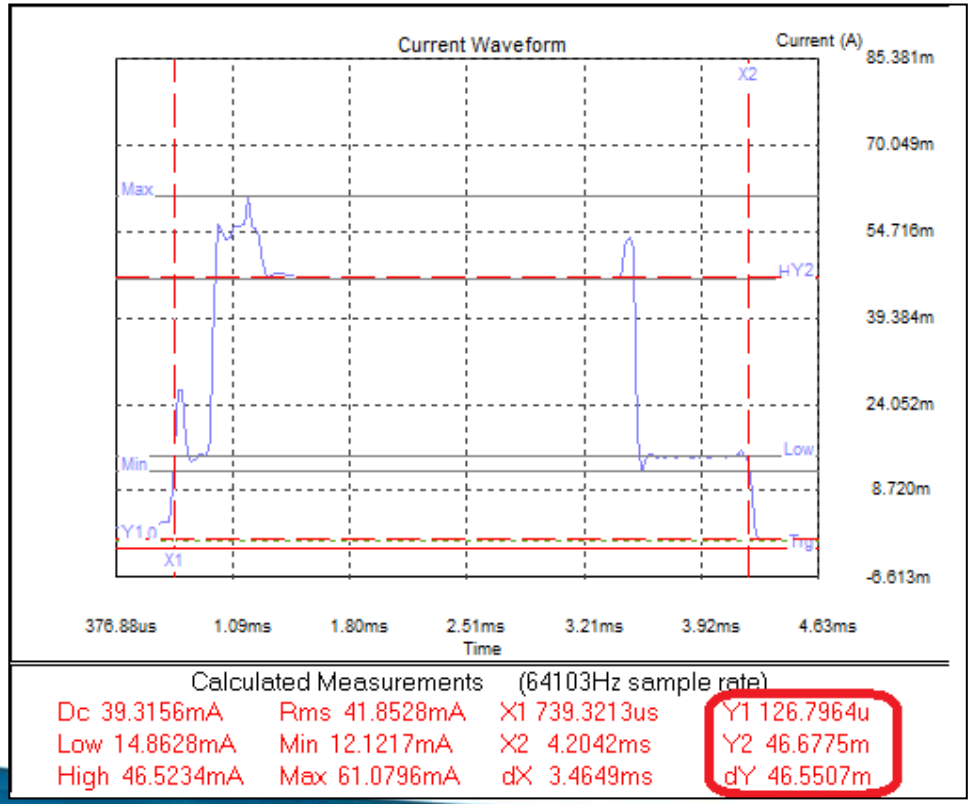
Pin Map (UM0120)

```
const PMAP_TypeDef pmap_func[]=
{
//   Pin Name      Func Select              Func PU/PD       Slp PU/PD        DrvStrenth
     {_PA_14,      PINMUX_FUNCTION_SWD,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SWD_CLK
     {_PA_15,      PINMUX_FUNCTION_SWD,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SWD_DATA
     {_PA_13,      PINMUX_FUNCTION_PWM,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //PWM4
     {_PA_0,       PINMUX_FUNCTION_PWM,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //PWM2
     {_PA_16,      PINMUX_FUNCTION_PWM,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //PWM1
     {_PA_17,      PINMUX_FUNCTION_PWM,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //PWM2
     {_PA_25,      PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART1_RXD
     {_PA_26,      PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART1_TXD
     {_PA_28,      PINMUX_FUNCTION_I2C,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2C1_SCL
     {_PA_27,      PINMUX_FUNCTION_I2C,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2C1_SDA
     {_PA_12,      PINMUX_FUNCTION_PWM,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //PWM3
     {_PA_4,       PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART0_TXD
     {_PA_1,       PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART0_RXD
     {_PA_3,       PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART0_RTS
     {_PA_2,       PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART0_CTS
     {_PA_6,       PINMUX_FUNCTION_SPIF,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPIC_CS
     {_PA_7,       PINMUX_FUNCTION_SPIF,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPIC_DATA1
     {_PA_8,       PINMUX_FUNCTION_SPIF,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPIC_DATA2
     {_PA_9,       PINMUX_FUNCTION_SPIF,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPIC_DATA0
     {_PA_10,      PINMUX_FUNCTION_SPIF,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPIC_CLK
     {_PA_11,      PINMUX_FUNCTION_SPIF,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPIC_DATA3
     {_PA_5,       PINMUX_FUNCTION_PWM,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //PWM4
     {_PA_18,      PINMUX_FUNCTION_SDIOD,   GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SD_D2
     {_PA_19,      PINMUX_FUNCTION_SDIOD,   GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SD_D3
     {_PA_20,      PINMUX_FUNCTION_SDIOD,   GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SD_CMD
     {_PA_21,      PINMUX_FUNCTION_SDIOD,   GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SD_CLK
     {_PA_22,      PINMUX_FUNCTION_SDIOD,   GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SD_D0
     {_PA_23,      PINMUX_FUNCTION_SDIOD,   GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SD_D1
     {_PB_0,       PINMUX_FUNCTION_SPIM,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPI1_CS
     {_PB_1,       PINMUX_FUNCTION_SPIM,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPI1_CLK
     {_PB_2,       PINMUX_FUNCTION_SPIM,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPI1_MISO
     {_PB_3,       PINMUX_FUNCTION_SPIM,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //SPI1_MOSI
     {_PB_4,       PINMUX_FUNCTION_I2S,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2S_MCK
     {_PB_5,       PINMUX_FUNCTION_I2S,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2S_SD_TX
     {_PA_24,      PINMUX_FUNCTION_I2S,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2S_SD_RX
     {_PA_31,      PINMUX_FUNCTION_I2S,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2S_CLK
     {_PB_6,       PINMUX_FUNCTION_I2S,     GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //I2S_WS
     {_PA_30,      PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART2_log_TXD
     {_PA_29,      PINMUX_FUNCTION_UART,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //UART2_log_RXD
     {_PNC,        PINMUX_FUNCTION_GPIO,    GPIO_PuPd_NOPULL, GPIO_PuPd_NOPULL, PAD_DRV_STRENGTH_0}, //table end
};
```

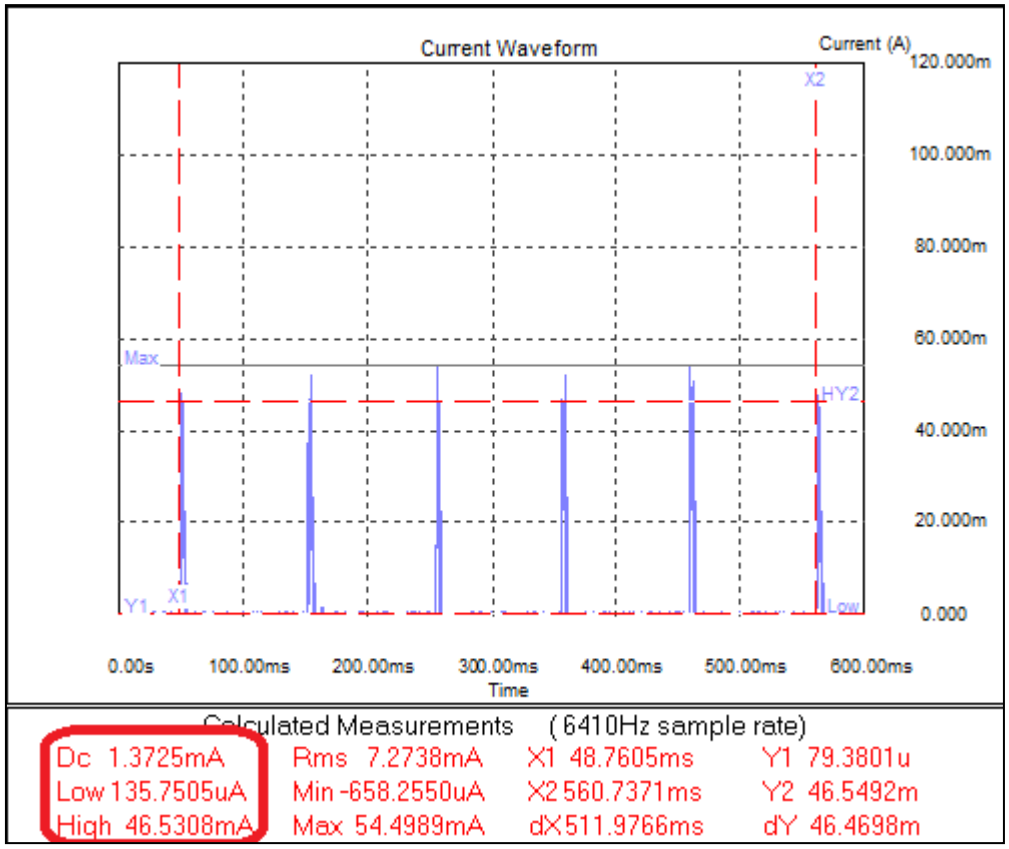
WIFI

WIFI

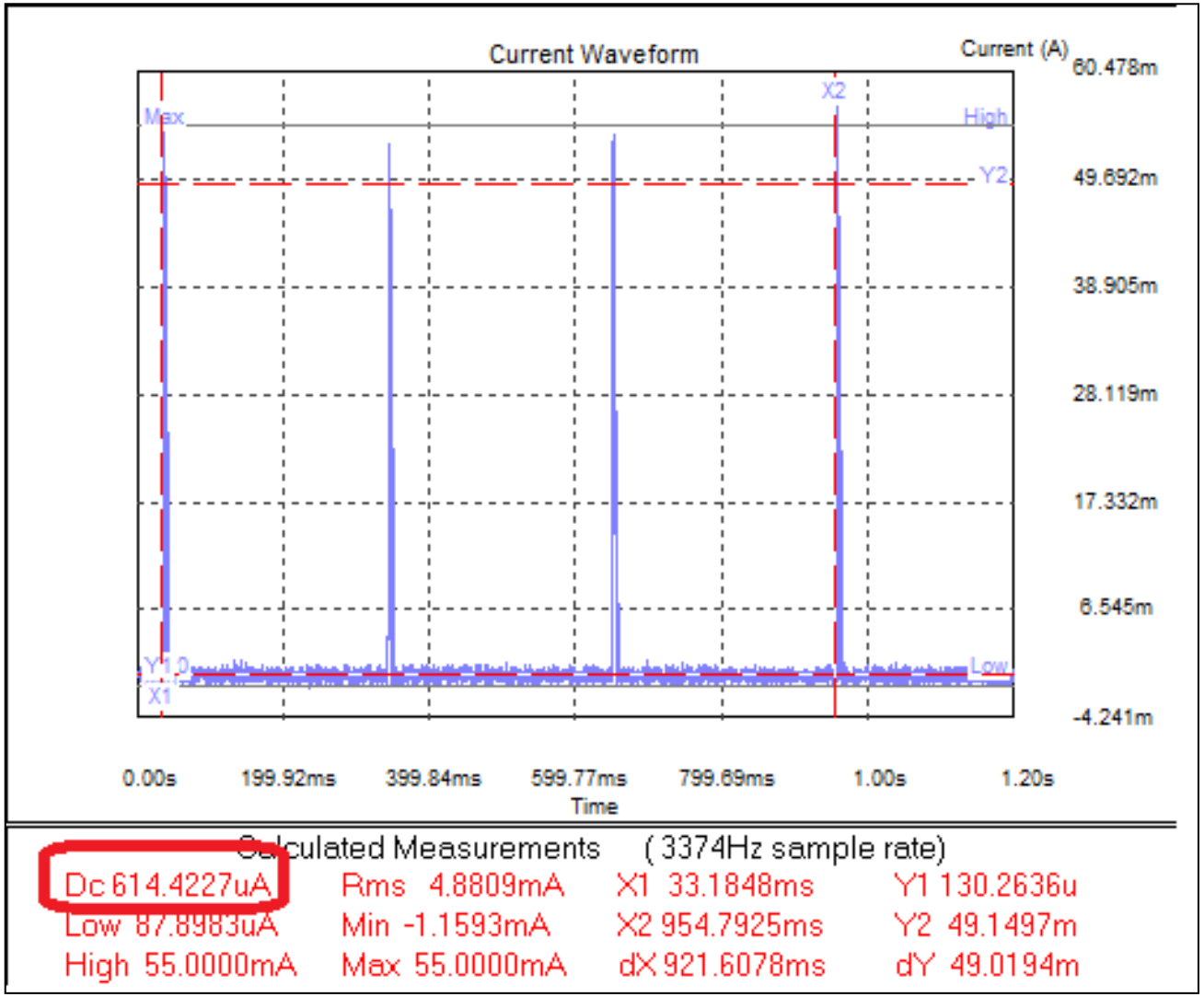
- Dedicated network processor for power saving
- WIFI can receive beacon & data periodically with CM4 in sleep mode
- Wakeup CM4 when needed (WOWLAN)



DTIM=1



DTIM=3



Power Saving Modes

SLEEP

Wakeup source	wakeup	comment
GPIO interrupt	YES	High/Low active
general purpose timer	YES	TIM4/TIM5
wlan	YES	
ADC	YES	
UART	YES	
I2C	YES	
SDIO/GSPI	YES	
USB	YES	
Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
RTC	YES	
System timer	YES	
low precision timer	YES	

DSTANDBY

Wakeup source	wakeup	comment
Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23
RTC	YES	
System timer	YES	
low precision timer	YES	

DSLEEP

Wakeup source	wakeup	comment
low precision timer	YES	
Dsleep Wake pin	YES	GPIOA_5 GPIOA_18 GPIOA_22 GPIOA_23

Power Consumption

Power Mode

CPU	Dsleep	Dstandby	sleep
XXX_CPU	20uA	600uA	4mA
Ameba-I	20uA	52uA	906uA
8711BG(QFN68)	7.5uA	70uA	120uA
8711BN(QFN48)	7.5uA	70uA	120uA
8710BN(QFN32)	7.5uA	70uA	120uA

WIFI LPS

- CPU Sleep (WOWLAN)

	QFN68 (SWR)	QFN48 (SWR)	QFN32 (LDO)
DTIM=1	1.2mA	1.3mA	2.6mA
DTIM=3	587uA	614uA	1.1mA

- CPU Active

	QFN68 (SWR)	QFN48 (SWR)	QFN32 (LDO)
DTIM=1	23mA	23mA	47mA
DTIM=3	22uA	22uA	46mA

WIFI RX

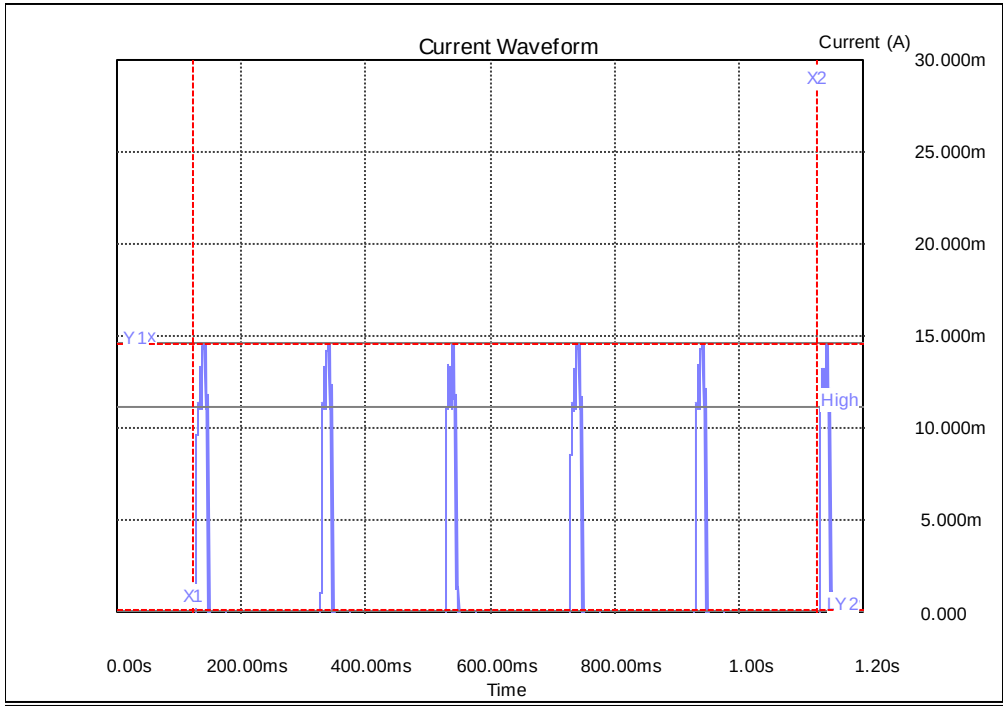
	QFN68 (SWR)	QFN48 (SWR)	QFN32 (LDO)
CPU Sleep	46mA	46mA	90mA
CPU Active	62mA	62mA	120mA

UART

Very Low Power Consumption

	Operation Mode	Baud Rate	Sleep Power Consumption
Ameba-Z	High speed mode	110bps~6Mbps	2.5 mA
	Low power mode	110bps~500Kbps	120 uA
Ameba-I	N/A	110bps~6Mbps	5.0 mA

Very Low Power Consumption



Calculated Measurements (3374Hz sample rate)

Dc 1.1978mA	Rms 3.6333mA	X1 123.7500ms	Y1 14.6101m
Low 145.3806uA	Min -35.6241uA	X2 1.1231s	Y2 155.9792u
High 11.2563mA	Max 14.6531mA	dX 0.9994s	dY -14.4541m

Enhanced Rx

Peer Rate	0%	-1%	-%1.5	-%2	-%2.5	-3%	-3.5%	-4.0%	-4.5%	-5.0%
	9600	9504	9456	9408	9360	9312	9264	9216	9168	9120
	38400	38016	37824	37632	37440	37248	37056	36864	36672	36480
	115200	114084	113472	112896	112320	111744	111168	110592	110016	109440
	460800	456192	453888	451584	449280	446976	444672	442368	440064	437760
RX	ok	ok	ok	ok	ok	ok	ok	ok	ok	fail

Log-UART

- LOGUART is a regular UART
  - Low power RX not supported
  - High speed supported

I2C

I2C

- DMA mode Supported
- Power save

Operation mode	CM4 sleep	Wakeup method
Slave mode	Y	address match wakeup
Master mode	Y	GPIO wakeup

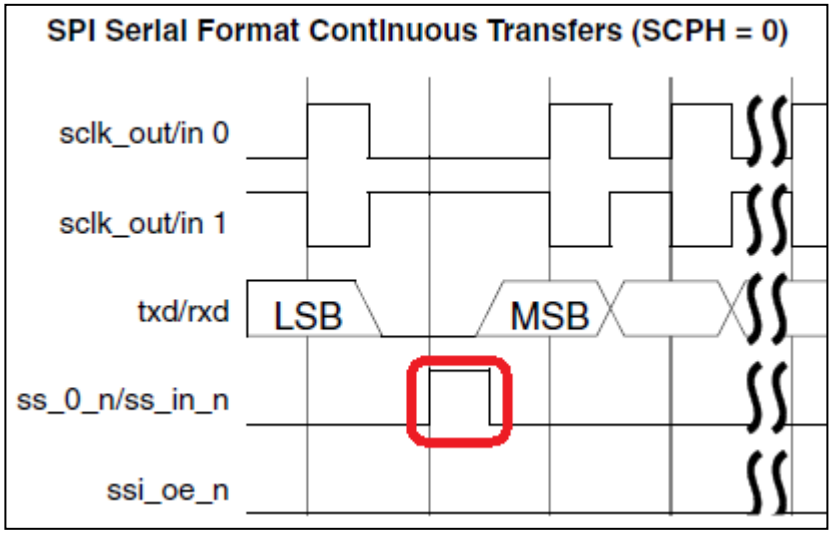
- Speed mode

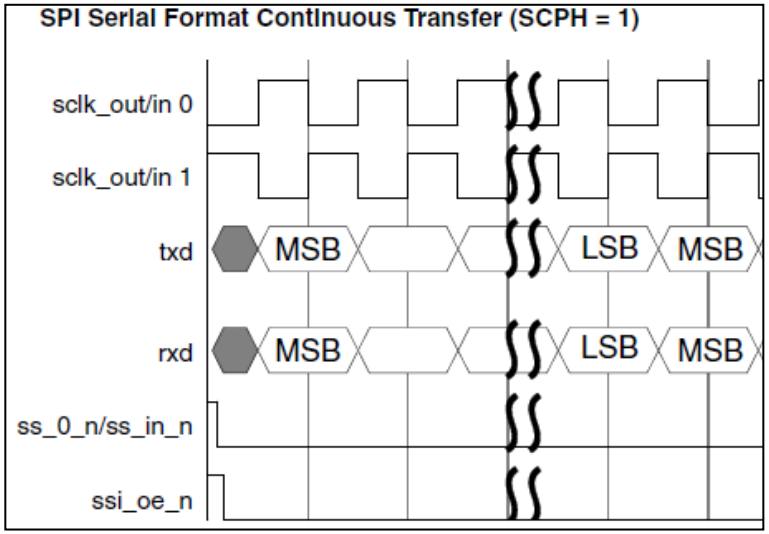
Speed mode	speed	supported
standard	100K	Y
fast	400K	Y
High speed	3.4M	N

SPI

SPI Master

- Max. 30MHz
- HW control CS
  - CS0 only
  - CS will toggle for continuous transfer when CPHA=0

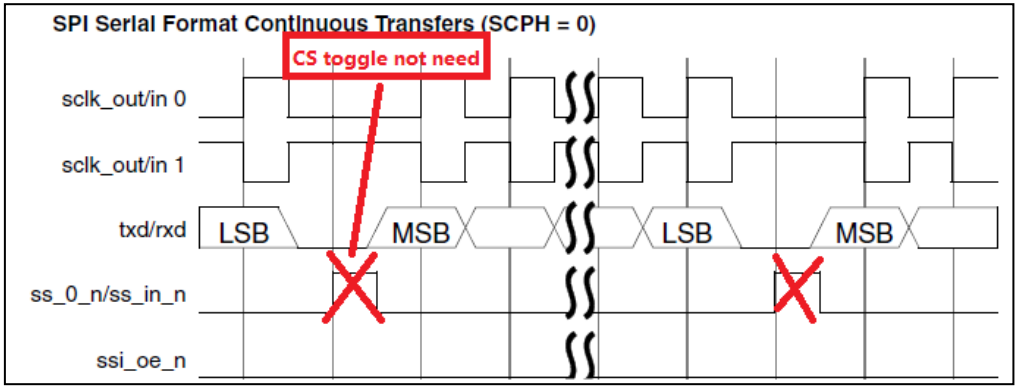


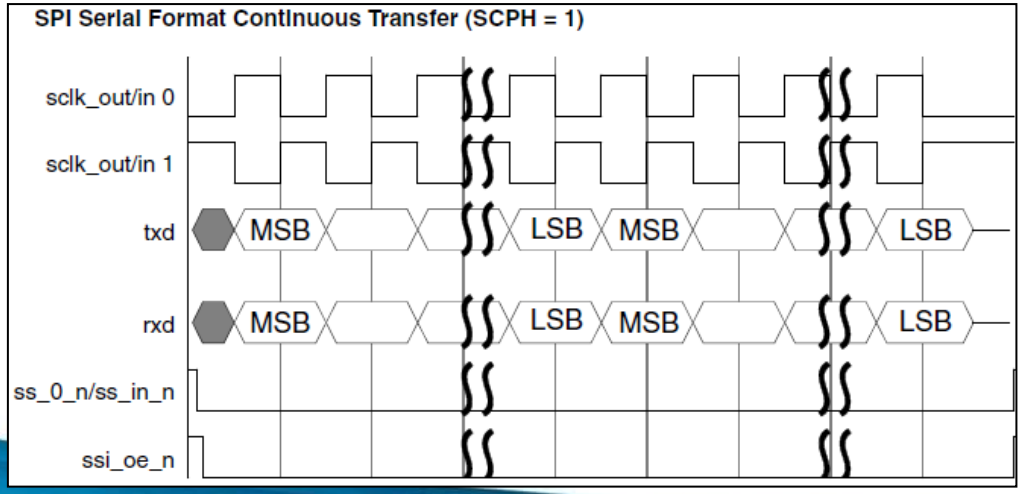


- SW control CS
  - Up to 8 CS pins are supported
  - CS behavior is configurable

SPI Slave

- Max. 30Mhz
- Compatible with STM SPI
  - CS needn't toggle for continuous transfer when CPHA=0





G-Timers and PWM

TIM0-TIM3-Counter

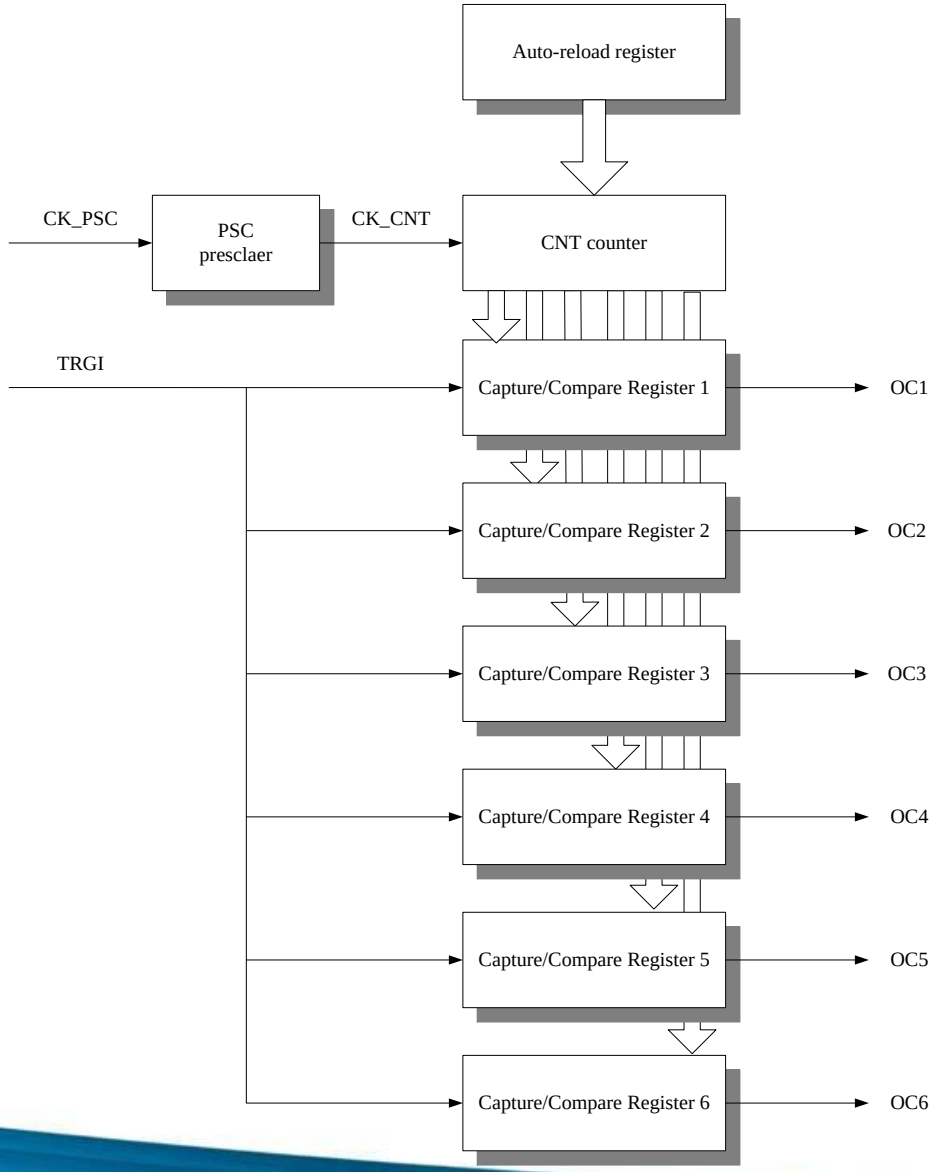
- TIM0: sys-timer for delay
- TIM3: ADC one shot mode(low power mode)

Name	TIM0/1/2/3
channels	1
clock source	32k
resolution	32bit
prescaler	-
counter mode	Up
one pulse mode	-
PWM mode with polarity selection	-
statistic pulse width	-
statistic pulse number	-
interrupt generation	●
DMA generation	-
input pin	-
output pin	-
Wakeup sleep mode	-

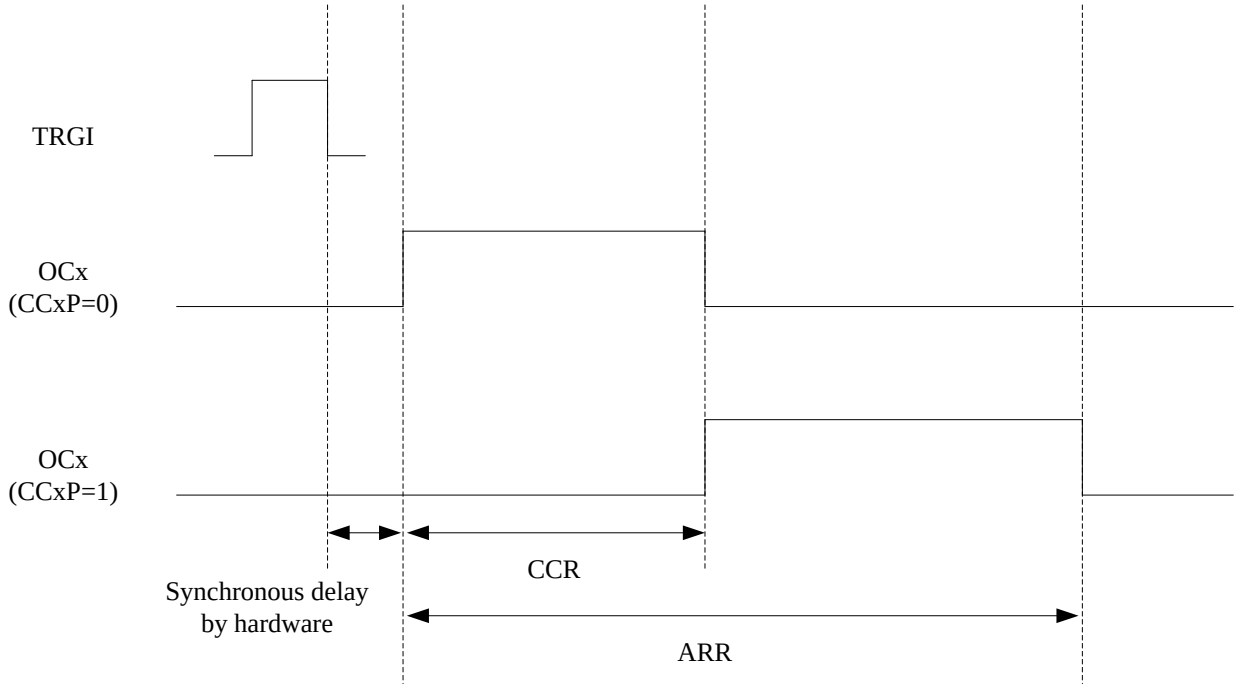
TIM5-PWM&Capture

Name	TIM5
channels	6
clock source	XTAL
resolution	16bit
prescaler	8bit
counter mode	Up
one pulse mode	●
PWM mode with polarity selection	●
statistic pulse width	-
statistic pulse number	-
interrupt generation	●
DMA generation	●
input pin	1 input capture
output pin	6 PWM out
Wakeup sleep mode	●

TIM5-PWM&Capture



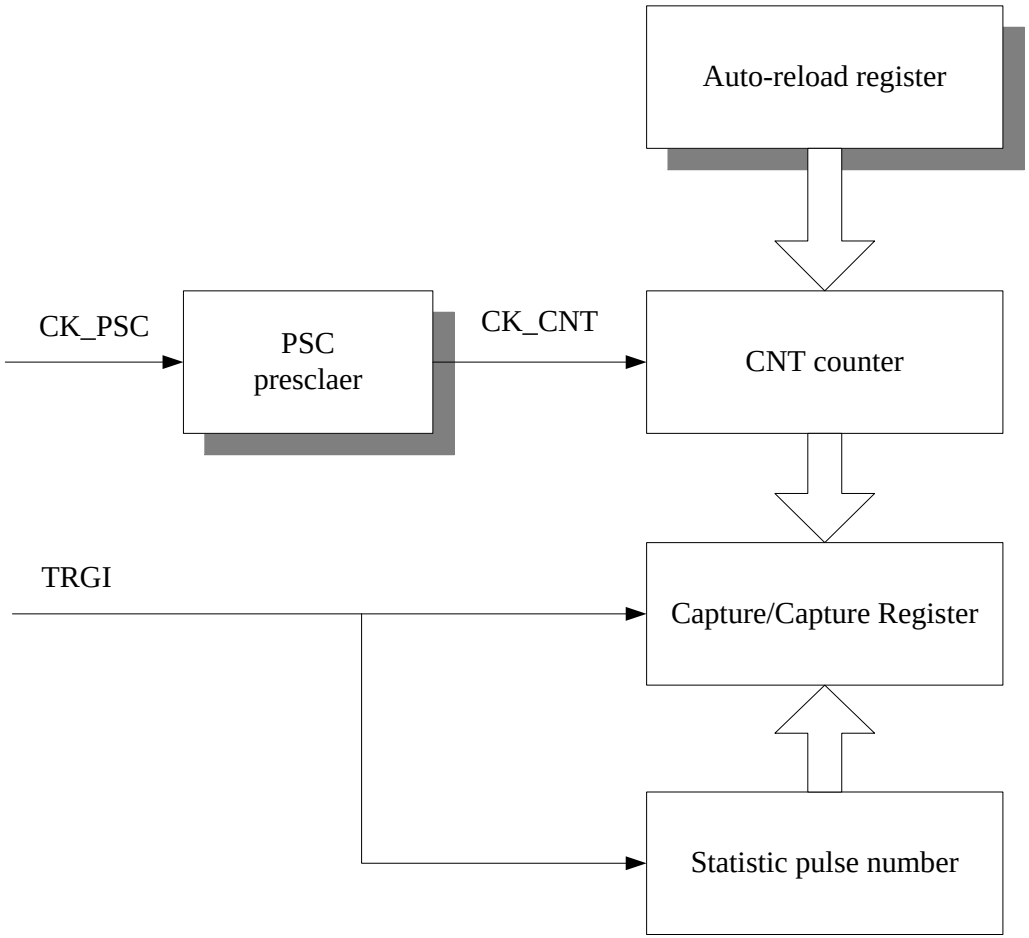
TIM5-one pulse



TIM4-Capture

Name	TIM4
channels	1
clock source	XTAL
resolution	16bit
prescaler	8bit
counter mode	Up
one pulse mode	-
PWM mode with polarity selection	-
statistic pulse width	●
statistic pulse number	●
interrupt generation	●
DMA generation	●
input pin	1 input capture
output pin	-
Wakeup sleep mode	●

TIM4-Capture



RTC

HW RTC

- Clock source
  - XTAL 40M
  - NCO 32K
  - EXT 32K
- Time with S/M/H/D
  - Hours: 12 or 24-hour format.
  - Days: 0~0x1FF
- Daylight saving
  - Compensation programmable by software.

HW RTC

- Alarm with interrupt mask:
  - seconds
  - minutes
  - hours
  - Days
- Power save

	RTC reset	wakeup
Power off	Y	NA
Reset	Y	NA
Deep sleep	Y	NA
Deep standby	N	Y
sleep	N	Y

HW RTC

- RTC OUT
  - Alarm output
  - clock output is clk_spre (default: 1Hz)
  - clock output is clk_apre (default: 512 Hz)

BACKUP REG

Backup Register

- Size (4 dwords)
  - Byte[0]: reserved for system
  - Byte[15:1]: Available for user
- byte0:
  - BIT(0): HW bit, watchdog reset or system reset happen
  - BIT(1): HW bit, BOR2 happen
  - BIT(2): SW bit, reserved
  - BIT(3): ROM bit, reserved for UART download
  - BIT(4): ROM bit, reserved for UART download
  - BIT(5): SW bit, reserved
  - BIT(6): HW bit, BOR2 Temp register
  - BIT(7): HW bit, BOR2 detection enable

Backup Register

- Reset

	Reset
Power off	Y
Reset button	Y
Deep sleep	Y
Vector reset	N
System reset	N
Deep standby	N
sleep	N

USB Device

USB device

- USB2.0 device only
- INIC mode
  - WIFI stack offload
  - Low performance
- Dongle mode
  - WIFI stack isn't offloaded
  - High performance with around 100Mbps throughput

ADC

ADC

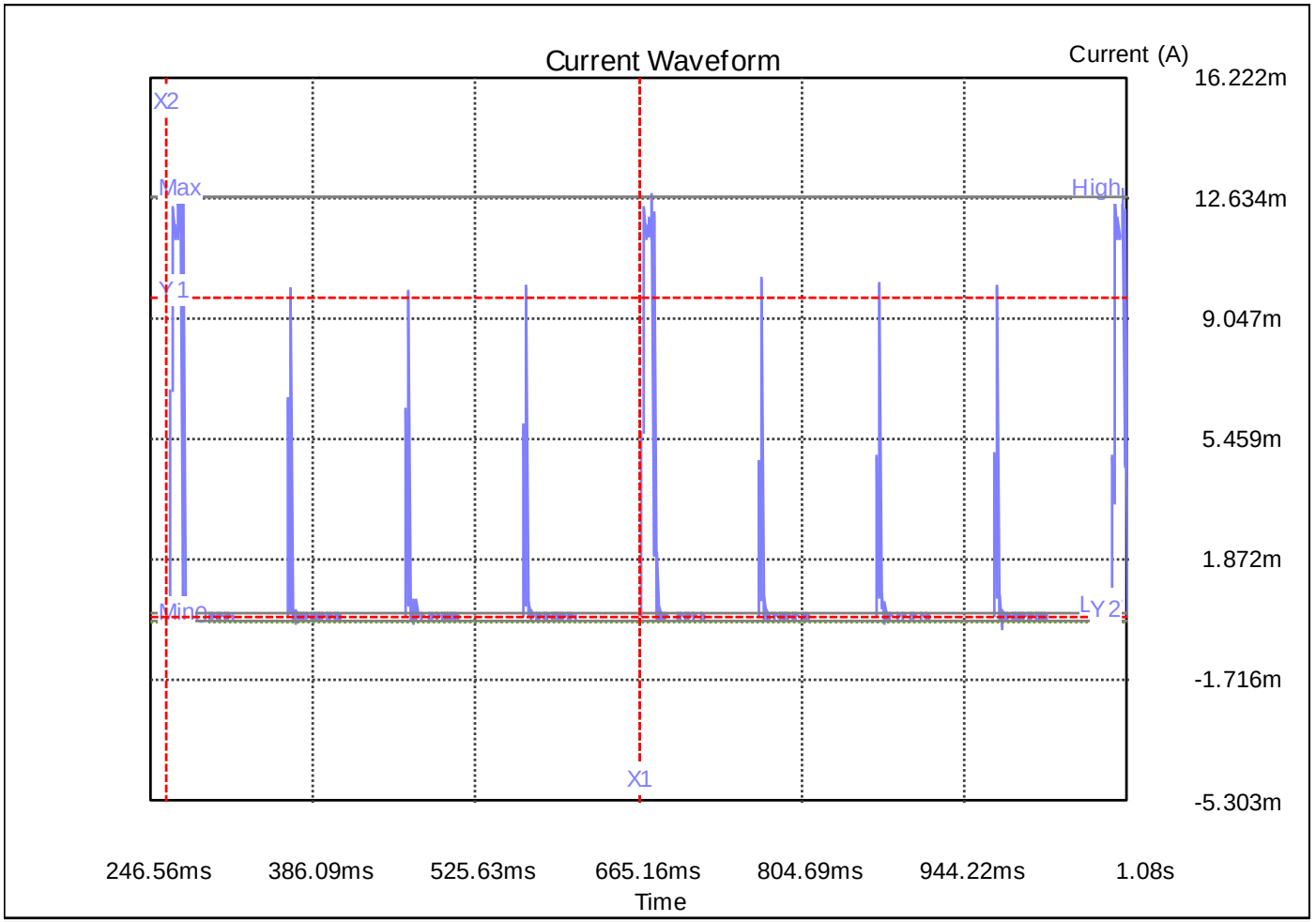
- Features

	internal	Thermal	VBAT	Voltage	
CH0	Y	Y	N/A	N/A	
CH1	N	N	N	0-3V	
CH2	N	N	Y	0-5V	
CH3	N	N	N	0-3V	

ADC Power save

- One shot mode
  - ADC periodically samples data with CM4 in sleep mode
  - TIM3 is used
- Wakeup
  - ADC will wakeup CM4 when the threshold of RXFIFO reaches

ADC Power consumption

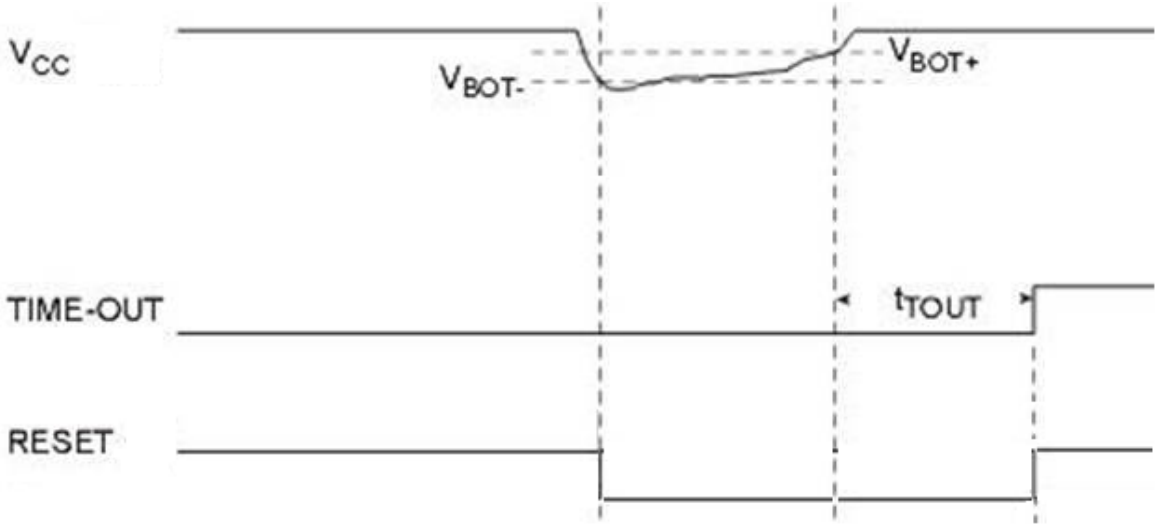


Calculated Measurements (3374Hz sample rate)

Dc 738.3929uA	Rms 2.1044mA	X1 665.1562ms	Y1 9.6934m
Low 315.5780uA	Min 94.6646uA	X2 260.9517ms	Y2 143.2738u
High 12.6935mA	Max 12.6935mA	dX 404.2046ms	dY -9.5501m

BOR

BOR1

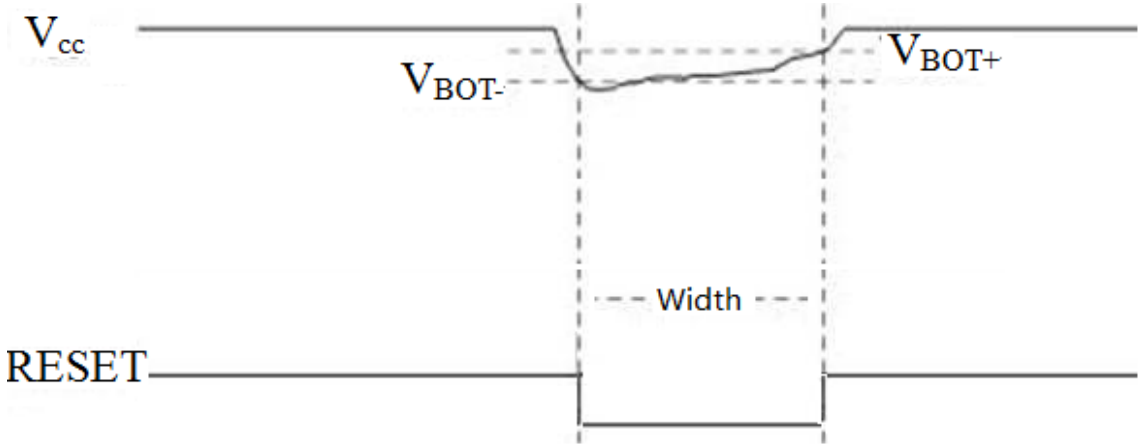


	Value
V_{BOT-}	2.5V
V_{BOT+}	2.7V
t_{TOUT}	1ms

BOR1 Operation Mode

Operation Mode	Support
Interrupt mode	N
Reset mode	Y

BOR2



	Value
V_{BOT-}	3.0V (±5%)
V_{BOT+}	3.1V (±5%)
Width	>100ns

BOR2 Operation Mode

Operation Mode	Support	ENABLE	BOR2 Action
Interrupt mode	Y	0x138[7]=0 0x100[30]=1	SYSIRQ 0x108[30]=1
Reset mode	Y	0x138[7]=1	Digital Reset 0x138[1]=1

Digital Domain Global Reset

Functions	Reset
Backup Register	N
RTC	N
CPU	Y
Register	Y
SRAM	Y
Peripherals	Y

Thank You!

Realtek is committed to providing its customers with the best possible connectivity and multimedia solutions.