



# Ameba-Z EFUSE Calibration Data Spec

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**Version: 0.1**

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## Modification History

Version	Date	Author	Change
0.1	2016/11/16	Chaoming_li	Initial version.

# 1. Calibration Data Spec

- Total 512 bytes:

Bytes	Contents	Description	Value																												
00h	95h	These 2 bytes contain the ID code word for the <i>RTL8195A</i> . The <i>RTL8195A</i> will load the contents of the eFuse into the corresponding location if the ID word is correct.	8195h																												
01h	81h																														
02h ~ 1Fh	Reserved	Reserved for Realtek. Do not change this field without Realtek's approval.	-																												
20h	Path A 2.4G CCK-1TX Power Index (Absolute Value)	Path A CCK Power Index for Ch 1,2, Range 0~63.	2Dh																												
21h		Path A CCK Power Index for Ch 3, 4, 5, Range 0~63.	2Dh																												
22h		Path A CCK Power Index for Ch 6, 7, 8, Range 0~63.	2Dh																												
23h		Path A CCK Power Index for Ch 9, 10, 11, Range 0~63.	2Dh																												
24h		Path A CCK Power Index for Ch 12, 13, Range 0~63.	2Dh																												
25h		Path A CCK Power Index for Ch 14, Range 0~63.	2Dh																												
26h		Path A 2.4G BW40-1S TX Power Index (Absolute Value)	Path A 2G BW40-1S Power Index for Ch 1, 2, Range 0~63.	2Dh																											
27h	Path A 2G BW40-1S Power Index for Ch 3, 4, 5, Range 0~63.		2Dh																												
28h	Path A 2G BW40-1S Power Index for Ch 6, 7, 8, Range 0~63.		2Dh																												
29h	Path A 2G BW40-1S Power Index for Ch 9, 10, 11, Range 0~63.		2Dh																												
2Ah	Path A 2G BW40-1S Power Index for Ch 12, 13, 14 Range 0~63.		2Dh																												
2Bh	Path A 2.4G BW20-1S TX Power Index Difference OFDM-1 TX Power Index Difference	Power Index Difference between BW20-1S and BW40-1S. Bit[7:4] : Path A 2G Offset, Range -8~7. Power Index Difference between OFDM-1Tx and BW40-1S. Bit[3:0] : Path A 2G Offset, Range -8~7.	02h																												
2Ch~C7h	Reserved	Reserved for Realtek.	-																												
C8h	Channel Plan	Bit[7]: Software configure mode 0h: Enable software configure( refer to Channel Plane Domain Code) 1h: Disable software configure( can't change Channel Plan Setting) Bit[6:0]: Channel Plan <table border="1" data-bbox="571 1608 1289 1848"> <thead> <tr> <th>Domain Code</th> <th>Value</th> <th>Channels</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2G_WORLD</td> <td>20h</td> <td>1~13</td> <td>Worldwird 13</td> </tr> <tr> <td>2G_ETSI1</td> <td>21h</td> <td>1~13</td> <td>Europe 2G</td> </tr> <tr> <td>2G_FCC1</td> <td>22h</td> <td>1~11</td> <td>US 2G</td> </tr> <tr> <td>2G_MKK1</td> <td>23h</td> <td>1~13, 14</td> <td>Japan 2G</td> </tr> <tr> <td>2G_ETSI2</td> <td>24h</td> <td>10~13</td> <td>France 2G</td> </tr> <tr> <td>2G_FCC2</td> <td>2Ah</td> <td>1~13</td> <td>US 2G</td> </tr> </tbody> </table>	Domain Code	Value	Channels	Description	2G_WORLD	20h	1~13	Worldwird 13	2G_ETSI1	21h	1~13	Europe 2G	2G_FCC1	22h	1~11	US 2G	2G_MKK1	23h	1~13, 14	Japan 2G	2G_ETSI2	24h	10~13	France 2G	2G_FCC2	2Ah	1~13	US 2G	20h
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C9h	Crystal Calibration	XTAL_K Value Bit[5:0], Xi=Xo Range 0~3F h. Bit[7:6]: reserved FF h = 00 h	20h																												

Bytes	Contents	Description	Value								
CAh	Thermal Meter	Thermal Meter Default Value System maker will calibrate a value and save it in calibration data section . Bit[7:0]: Thermal Meter Value	1Ah								
CBh	Reserved	Reserved for Realtek	05h								
CCh	Reserved	Reserved for Realtek.	00h								
CDh	Reserved	Reserved for Realtek.	00h								
CEh	Reserved	Reserved for Realtek.	00h								
CFh	Reserved	Reserved for Realtek.	FFh								
D0h	CCCR	Bit[0]: SCSI ,CCCR 0x07[6] Bit[1]:SDC , CCCR 0x08[0] Bit[2]:SMB , CCCR 0x08[1] Bit[3]:S4MI , CCCR 0x08[4] Bit[4]:SMPC , CCCR 0x12[0] Bit[5]:SHS , CCCR 0x13[0] Bit[6]:SSDR50 , CCCR 0x14[0] Bit[7]:SSDR104 , CCCR 0x14[1]	3Eh								
D1h	CCCR&FBR	Bit[0]:SDDR50 , CCCR 0x14[2] Bit[1]:SDTA , CCCR 0x15[0] Bit[2]:SDTC , CCCR 0x15[1] Bit[3]:SDTD , CCCR 0x15[2] Bit[4]:SAI , CCCR 0x16[0] Bit[5]: Init_skip, 0:need cmd 0 5 5 3 7 to enable Wifi ,(default) 1:skip Bit[6~7]:reserve	00h								
D2h		Bit[0]: SPS ,FBR 0x102[0] Bit[1~3]:reserved Bit[4~7]:PS3 ,FBR 0x102[4~7]	01h								
D3h	CCCR	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7:4</td> <td>Reserved</td> </tr> <tr> <td>3:0</td> <td>CCCR Format Version number 0x02: CCCR/FBR Version 2.00</td> </tr> </tbody> </table>	Bit	Description	7:4	Reserved	3:0	CCCR Format Version number 0x02: CCCR/FBR Version 2.00	02h		
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D4h	SDIO_MODE	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7:4</td> <td><b>SDx</b>: SD Format Version number 0x02: SD physical Specification Version 2.00</td> </tr> <tr> <td>3:0</td> <td><b>SDIOx</b>: SDIO Format Version number 0x03: SDIO physical Specification Version 2.00</td> </tr> <tr> <td colspan="2"><b>Note</b>: SDIOx and SDx are in CCCR register.</td> </tr> </tbody> </table>	Bit	Description	7:4	<b>SDx</b> : SD Format Version number 0x02: SD physical Specification Version 2.00	3:0	<b>SDIOx</b> : SDIO Format Version number 0x03: SDIO physical Specification Version 2.00	<b>Note</b> : SDIOx and SDx are in CCCR register.		23h
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3:0	<b>SDIOx</b> : SDIO Format Version number 0x03: SDIO physical Specification Version 2.00										
<b>Note</b> : SDIOx and SDx are in CCCR register.											
D5h~D7h	OCR	OCR value. Little Endian order. ( This value must be consistent with CIS tuple value )	FC0000h								
D8h~DBh	Common CIS Data	Offset 68h~6Bh: CISTPL_MANFID Value :0x20 04 4C 02									

Bytes	Contents	Description	Value
DCh~DDh	Common CIS Data	8195AM Offset 6Ch~6Dh: CISTPL_MANFID Value : <b>95 81</b> 8711AF Offset 6Ch~6Dh: CISTPL_MANFID Value : <b>11 87</b>	
DEh~E8h	Common CIS Data	Offset 6Eh~71h: CISTPL_FUNCID Value :21 02 0C 00 Offset 72h~78h: CISTPL_FUNCE Value :22 04 00 08 00 32 FF	
E9h~119h	Function 1 CIS Data	Offset 79h~7Ch: CISTPL_FUNCID Value :21 02 0C 00 Offset 7Dh~7Eh:CISTPL_FUNCE Value :22 2A Offset 7Fh~A9h: Value : 01 01 00 00 00 00 00 00 - 00 00 00 00 00 02 00 FF FF 00 00 00 00 00 00 00 - 00 00 00 00 00 00 00 00 00 00 EB 00 6E 01 00 00 - 00 00 FF	
11Ah~11Fh	Function 1 CIS Data MAC Address	MAC Address: After the auto-load command or hardware reset, the <i>RTL8195A</i> loads MAC Addresses to MACID of the I/O registers of the <i>RTL8195A</i> .	FFFFFFF FFFFFFh
120h~130h	Reserved	Reserved for Realtek.	FFh
131h	Board Options	Bit[2:0]: Regulatory selection. 0h: driver-defined maximum power offset for longer communication range. (refer to Power by rate table) 1h: Power limit table-defined maximum power offset range (refer to Power by rate table and Power limit table to take the smaller index value) 2h: not support power offset by rate (Don't refer to Power by rate table) 3h~7h: reserved Bit[3]: reserved  Bit[4]: reserved  Bit[7:5]: reserved .	01h

Bytes	Contents	Description	Value
132h	Feature Options	<p>Bit[1:0]: function configuration of pin_LED0 and pin_LED1</p> <p>Bit[3:2]: Link Speed shown in OS            0h: Current Tx PHY Rate            1h: Current Rx PHY Rate            2h: Maximum RX PHY Rate            3h: reserved</p> <p>Bit[4]: power down mode selection            0: radio off            1: power down</p> <p>Bit[5]: Enable bluetooth coexistence            0: Disable            1: Enable</p> <p>Bit[6]: Enable WoWLAN            0: Disable            1: Enable</p> <p>Bit[7]: Enable WAPI support            0: Disable            1: Enable</p>	00h
133h	Antenna Setting	<p>Bit[0]: Total antenna number            0: 2-Antenna (default)            1: 1-Antenna</p> <p>Bit[5:1]: reserved</p> <p>Bit[6]: Single antenna path            0: Single antenna use S1 (default)            1: Single antenna use S0</p> <p>Bit[7]: reserved</p>	10h
134h	Version	The EEPROM content version.	00h
135h	Customer ID	Customer ID (0x00 and 0xFF are reserved for Realtek)	FFh

Bytes	Contents	Description	Value
136h	2G Tx BB Swing Setting	Bit[1:0]: 2G PathA OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB Bit[3:2]: 2G PathB OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB Bit[5:4]: 2G PathC OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB Bit[7:6]: 2G PathD OFDM 0h: 0dB (default) 1h: -3dB 2h: -6dB 3h: -9dB	00h
137h	Reserved	Reserved for Realtek.	FFh
138h	Tx Power Calibrator Rate	Bit[0]: 2G 40M Tx Power Calibrator Rate. 0h : HT40, MCS7 64QAM (default) Bit[7:1]: reserved	00h
139h	TRx antenna Options	Bit[7:0]: reserved	00h
13Ah	RFE Type	Bit[6:0]: RF Front-end Type 0h~Fh: reserved 10h: reserved 11h: reserved 12h: SPDT with single antenna. 13h: reserved 14h~7Fh: reserved	FFh
13Bh	Country code	ISO 3166-1 Country code. Default 0xFFFF: Driver follows setting according to “0xC8 Channel Plan”	FFh
13Ch	Country code	ISO 3166-1 Country code. Default 0xFFFF: Driver follows setting according to “0xC8 Channel Plan”	FFh
13Dh~13Fh	Reserved	Reserved for Realtek.	FFh