Realtek Ameba1 Memory Layout

This document introduces usage of ROM, SRAM, SDRAM, and Flash partition.

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1 Memory Size

This table lists memory size for individual model.

Feature	RTL8195AM	RTL8711AM	RTL8711AF
Package	TFBGA98	QFN56	QFN48
Package Dimension	6x6mm	7x7mm	6x6mm
CPU	ARM Cortex M3 166MHz		
ROM	1MB	1MB	1MB
Flash	selectable	selectable	1MB
RAM	2MB + 512KB	2MB + 512KB	512KB

2 ROM

The address for ROM is 0x00000000~0x000FFFFF. ROM space is not opened for developer.

3 SRAM

The address for SRAM is 0x10000000~0x1006FFFF. In IAR project, source codes are located in SRAM by default.

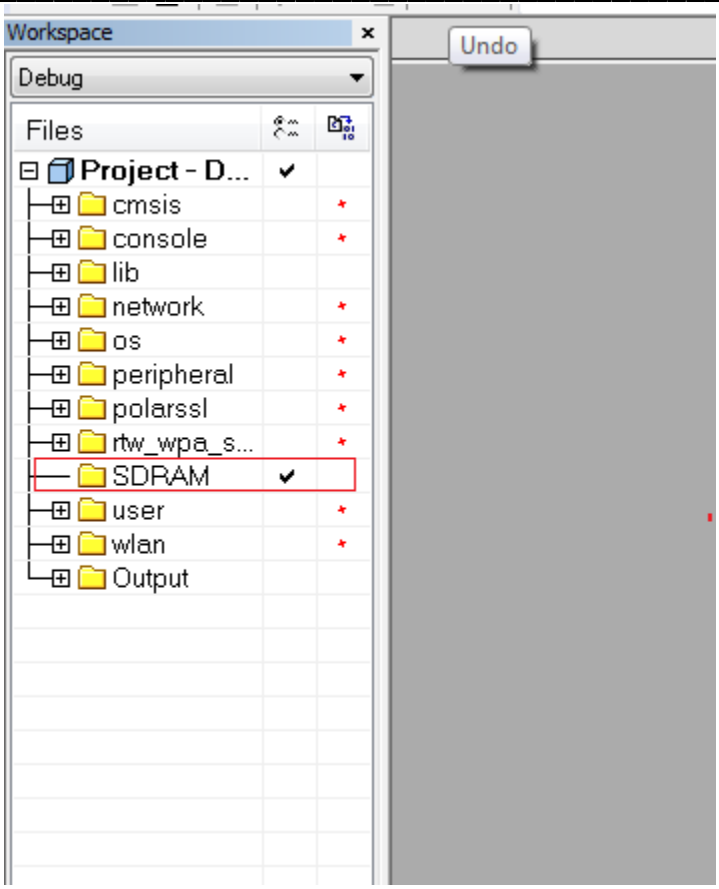
To check address of function call and data memory arranged by IAR, please refer to .map file after project build.

4 SDRAM

The address for SDRAM is 0x30000000~0x301FFFFF. Only RTL8195AM and RTL88711AM support 2MB SDRAM.

Put code in SDRAM

To use SDRAM, drag related code to the SDRAM folder in IAR project and rebuild project again.



To check address of function call and data memory arranged by IAR, please refer to .map file after project build.

Put data in SDRAM

Add a section name SECTION(".sdram.data") in front of the variable, then linker will locate the data in SDRAM.

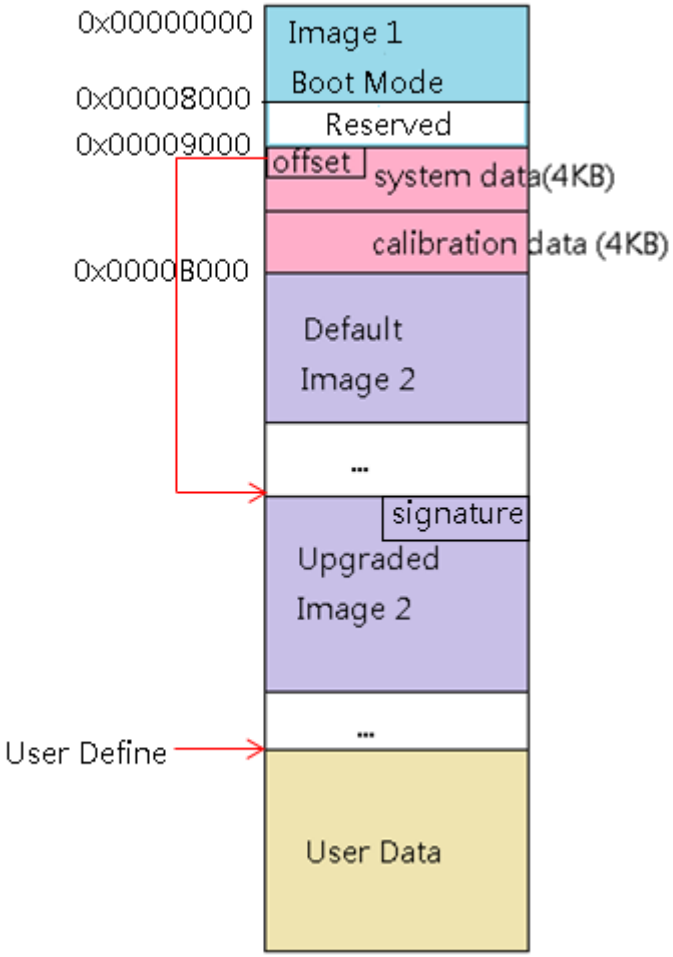
Ex:

SECTION(".sdram.data")

int value;

5 Flash

5.1 Flash Memory



The figure above is the flash memory layout.

5.1.1 Boot Loader (Image 1)

I. Fixed Address: 0x0000 ~ 0x7FFF, and its size is 32K。

II. Function: Hardware initialization, and Image 2 Firmware loading。

III. Image 1 Header:

- *Flash Calibration Pattern*: pattern for flash calibration: 16 bytes
  16 bytes fixed pattern is **99 99 96 96 3F CC 66 FC C0 33 CC 03 E5 DC 31 62**
- *Image Length:* The size of the image.
- *Image Address:* The SRAM /SDRAM address for the Image 1: 4 bytes
- *Image 2 Addr:* The starting address of Image 2 in Default Image 2: 2 bytes, unit is 1024 bytes.

IV. Image 1 format:

0x00	Flash Calibration Pattern			
0x10	Image Length	Image Address	(Image 2 Addr)/1024	Reserved
0x20 …	Firmware Code			

5.1.2 System Data

I. Flash memory address 0x9000 ~ 0xAFFF, total size is 8K

II. System Data (0x9000~0x9FFF): store system reserved data such as upgraded image 2 offset.

   i. Offset set (0x9000~0x9003): store the address of upgraded image 2.

III. Calibration Data (0xA000~0xAFFF): store the MP data such as RF calibration, AD calibration, …

5.1.3 Default Firmware (Default Image 2)

I. Flash memory address: Always start at 0xB000, size is variable.

II. Image 2 Header:

- *Image Length*: The size of this image 2: 4 bytes
- *Image Address*: The SRAM /SDRAM address for the Image.

III. The following figure shows the format of the image 2 :

0x00	Image Length	Image Address	Signature
0x10 …	Firmware Code		

5.1.4 Upgraded Firmware (Upgraded Image 2)

I. Image 2 memory layout:

0x00	Image Length	Image Address	Signature
0x10 …	Firmware Code		

- *Image Length*: The size of this image 2: 4 bytes
- *Image Address*: The SRAM /SDRAM address for the Image 2 is specified in this field.
- *Signature*: The boot loader reads this value to check the Upgraded image 2 is valid or not. “81958711” is for latest firmware and “01958711” is for older.

The decision policy for the boot loader to load the Default Firmware or the

Upgraded Firmware: The boot loader searches the upgraded image, if the signature value of Upgraded Firmware is valid, boot loader loads it to SRAM/SDRAM. Otherwise, the boot loader loads the Default Firmware.

5.1.5 Application Data

I. Flash memory address: the start address and the size is variable. The starting address and size of application data section is application dependent and is defined by individual user.
II. This section of flash memory is used by application.